MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

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| **Module Information**  **معلومات المادة الدراسية** | | | | | | | |
| **Module Title** | Computer Architecture | | | | **Module Delivery** | | |
| **Module Type** | Core | | | | * **☒ Theory** * **☐ Lecture** * **☐ Lab** * **☒ Tutorial** * **☐ Practical** * **☒ Seminar** | | |
| **Module Code** | COAR211 | | | |
| **ECTS Credits** | 6 | | | |
| **SWL (hr/sem)** | 150 | | | |
| **Module Level** | | UGx11 2 | **Semester of Delivery** | | | | 1 |
| **Administering Department** | | Type Dept. Code | **College** | Type College Code | | | |
| **Module Leader** | Dr. Hassan Awheed | | **e-mail** | Hassan.a.jeiad@uotechnology.edu.iq | | | |
| **Module Leader’s Acad. Title** | | Assist. Prof. | **Module Leader’s Qualification** | | | | Ph.D. |
| **Module Tutor** | Dr. Omar Nowfal | | **e-mail** | [omar.n.mohammedtaher@uotechnology.edu.iq](mailto:omar.n.mohammedtaher@uotechnology.edu.iq) | | | |
| **Peer Reviewer Name** | | 1.Dr. Rand Ali  2.Dr. Sama Salam. | **e-mail** | [rand.a.abdulhussain@uotechnology.edu.iq](mailto:rand.a.abdulhussain@uotechnology.edu.iq)  sama.s.samaan@uotechnology.edu.iq | | | |
| **Scientific Committee Approval Date** | |  | **Version Number** | | | 1.0 | |

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| **Relation with other Modules**  **العلاقة مع المواد الدراسية الأخرى** | | | |
| **Prerequisite module** | Digital System Design | **Semester** |  |
| **Co-requisites module** | None | **Semester** |  |

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| **Module Aims, Learning Outcomes and Indicative Contents**  **أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية** | |
| **Module Objectives**  **أهداف المادة الدراسية** | 1. To knowledge the basic concepts of computer architecture and organization. 2. To explain the considerations behind the design of basic computer systems. 3. To familiarize the basic CPU organization. 4. To help students in understanding various memory devices. 5. To facilitate students in learning IO communication. |
| **Module Learning Outcomes**  **مخرجات التعلم للمادة الدراسية** | 1. Understand the various components of computer and their interconnection. 2. Exploit the register transfer language to design basic digital systems. 3. Develop basic arithmetic and logical unit. 4. Identify the basic components and design of the elementary CPU with its ALU and control unit. 5. Develop basic computer system with integrating its various components. 6. Recognize the stack organization, instruction formats, addressing modes and RISC. 7. Develop memory system by select various memory devices as per requirement. 8. Identify the organization and performance issues of cache memory and virtual memory. 9. Recognize how the various types of IO mapping approaches applied in the computer system. 10. Identify the internal structure of PPI, DMA, and UART. 11. Understand the interaction between CPU and IOP. |
| **Indicative Contents**  **المحتويات الإرشادية** | Indicative content includes the following.  REGISTER TRANSFER AND MICRO-OPERATIONS:  Register Transfer Language, Register Transfer, Bus and Memory Transfers, Arithmetic, Logic, and Shift Micro-Operations, Arithmetic logic shift unit. [6 hrs]  BASIC COMPUTER ORGANIZATION AND DESIGN:  Instruction codes, Computer Registers, Computer Instructions and Instruction cycle. Timing and Control, Memory-Reference, Register-Reference, and IO-Reference Instructions, Input-Output and interrupt, Design of basic computer system. [8 hrs]  CENTRAL PROCESSING UNIT:  Stack organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Complex Instruction Set Computer (CISC) Reduced Instruction Set Computer (RISC), CISC vs RISC. [4 hrs]  MEMORY SYSTEM:  Memory Hierarchy, Semiconductor Memories, RAM, ROM, design of memory as per requirement. Associative memory, match logic derivation. Cache Memory and Performance considerations. Virtual memory. Replacement algorithms. [8 hrs]    INPUT OUTPUT:  I/O interface, Programmed IO, Memory Mapped IO, Interrupt Driven IO, PPI, DMA, UART, interaction between CPU and IOP. [4 hrs] |

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| **Learning and Teaching Strategies**  **استراتيجيات التعلم والتعليم** | |
| **Strategies** | The main leaning and teaching strategies can be summarized by:   1. **Lectures:** the instructor will present in-class lectures to introduce and clarify important concepts, theories, and principles related to the computer architecture. 2. **Interactive Discussions**: Engaging students in interactive discussions to encourage critical thinking. 3. **Use of Visuals and Multimedia:** Incorporating visual aids, multimedia resources, and interactive tools can enhance understanding and engagement. 4. **Assessment and Feedback**: Regular assessments, including quizzes, tests, and examinations to show how well the students understand the subject. |

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| **Student Workload (SWL)**  **الحمل الدراسي للطالب محسوب لـ ١٥ أسبوعا** | | | |
| **Structured SWL (h/sem)**  **الحمل الدراسي المنتظم للطالب خلال الفصل** | 63 | **Structured SWL (h/w)**  **الحمل الدراسي المنتظم للطالب أسبوعيا** | 4 |
| **Unstructured SWL (h/sem)**  **الحمل الدراسي غير المنتظم للطالب خلال الفصل** | 87 | **Unstructured SWL (h/w)**  **الحمل الدراسي غير المنتظم للطالب أسبوعيا** | 6 |
| **Total SWL (h/sem)**  **الحمل الدراسي الكلي للطالب خلال الفصل** | **150** | | |

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| **Module Evaluation**  **تقييم المادة الدراسية** | | | | | |
| **As** | | **Time/Number** | **Weight (Marks)** | **Week Due** | **Relevant Learning Outcome** |
| **Formative assessment** | **Quizzes** | 2 | 5% (10) | 5 and 10 | LO #1-#5 and #6-#8 |
| **Online Assignments** | 2 | 5% (10) | 6 and 11 | LO #2-#5 and #6-#8 |
| **Onsite assignment** | 4 | 5% (10) | 4,7,10,13 | All |
| **Midterm Exam** | 1hr | 10% (10) | 8 | LO #1 - #7 |
| **Summative assessment** | **Final Exam** | 3hr | 50% (50) | 16 | All |
| 100% (100 Marks) |  |  |  |  |

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| **Delivery Plan (Weekly Syllabus)**  **المنهاج الاسبوعي النظري** | |
| **Week** | **Material Covered** |
| **Week 1** | Introduction: general view on the computer architecture and organization. |
| **Week 2** | Register Transfer Language, Register Transfer, Bus and Memory Transfers. |
| **Week 3** | Arithmetic, Logic, and Shift Micro-Operations, Arithmetic logic shift unit. |
| **Week 4** | Instruction codes, Computer Registers. |
| **Week 5** | Computer Instructions and Instruction cycle. Timing and Control. |
| **Week 6** | Memory-Reference, Register-Reference, and IO-Reference Instructions. |
| **Week 7** | Input-Output and interrupt. Design of basic computer system. |
| **Week 8** | Mid-term Exam + Stack organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation. |
| **Week 9** | Complex Instruction Set Computer (CISC) Reduced Instruction Set Computer (RISC), CISC vs RISC. |
| **Week 10** | Memory Hierarchy, Semiconductor Memories, RAM, ROM, design of memory as per requirement. |
| **Week 11** | Associative memory, match logic derivation. |
| **Week 12** | Cache Memory and Performance considerations. |
| **Week 13** | Virtual memory. Replacement algorithms. |
| **Week 14** | I/O interface, Programmed IO, Memory Mapped IO, Interrupt Driven IO. |
| **Week 15** | PPI, DMA, UART, interaction between CPU and IOP. |
| **Week 16** | **Preparatory week before the final Exam** |

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| **Learning and Teaching Resources**  **مصادر التعلم والتدريس** | | |
|  | **Text** | **Available in the Library?** |
| **Required Texts** | M. Morris Mano, “Computer System Architecture”, Prentice-Hall of India, Pvt. Ltd., Third edition, 2007. | Yes |
| **Recommended Texts** | Mostafa Abd-El-Barr and Hesham El-Rewini, “Fundamentals of Computer Organization and Architecture”, John Wiley & Sons, 2005. | No |
| **Websites** |  | |

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| **Grading Scheme**  **مخطط الدرجات** | | | | |
| **Group** | **Grade** | **التقدير** | **Marks %** | **Definition** |
| **Success Group**  **(50 - 100)** | **A -** Excellent | **امتياز** | 90 - 100 | Outstanding Performance |
| **B -** Very Good | **جيد جدا** | 80 - 89 | Above average with some errors |
| **C -** Good | **جيد** | 70 - 79 | Sound work with notable errors |
| **D -** Satisfactory | **متوسط** | 60 - 69 | Fair but with major shortcomings |
| **E -** Sufficient | **مقبول** | 50 - 59 | Work meets minimum criteria |
| **Fail Group**  **(0 – 49)** | **FX –** Fail | **راسب (قيد المعالجة)** | (45-49) | More work required but credit awarded |
| **F –** Fail | **راسب** | (0-44) | Considerable amount of work required |
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| **Note:** Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above. | | | | |